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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,302	07/06/2001	Rajiv V. Joshi	YOR9-2001-0512US1 (728-21	5687

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/900,302	JOSHI ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5 and 7-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-5, and 7-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Receipt is acknowledged of the Amendment filed October 20, 2003.

Claim Objections

2. Claim 10 is objected to because of the following informalities: "the reverse of second input signals" on line 10 appears to be --the inverse of the second input signals--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation, "first and third transistors are PMOS transistors and the second transistor is a NMOS transistor" appears to be incorrect because the first transistor (444) receiving a first input signal is a NMOS transistor and the second transistor (442) receiving an inverse of the second input signal is a PMOS transistor as shown in Fig. 2C of the instant application. Rather the limitation should be --second and third transistors are PMOS transistors and the first transistor is a NMOS transistor--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-5, and 7-9 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sridhar et al. (US PAT No. 5,528,177). The response offers that for anticipation to be present each and every element of the claimed invention must be present in a single reference. The examiner agrees; hence:

<table>
<tr><td>Sridhar et al.

Fig. 2g (unless noted otherwise)</td><td>The claimed invention:</td></tr>
<tr><td>a logic circuit comprising 221,

222, 224</td><td>1. A MOSFET logic circuit for performing a logic

OR operation comprising:</td></tr>
<tr><td>221,

222</td><td>a first

and second transistors forming a transmission

gate</td></tr>
<tr><td>a signal at the node 231</td><td>for outputting an intermediate signal,</td></tr>
<tr><td>224 provides an output signal at the node 231 by combining the output of 221 and 222 with a signal being pulled up by 224 (see table below)

<table><tr><td>A</td><td>B</td><td>/B</td><td>231</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr></table></td><td>a third transistor for providing an output to be

combined with the intermediate signal to create

an output signal,</td></tr>
<tr><td>221 receives a first input signal, A,

224 receives the second input</td><td>the first transistor receiving a first input signal,

the third transistor receiving a second input</td></tr>
</table>

signal, /B, 222 receives B which is an inverse of /B	signal, the second transistor receiving an inverse of the second input signal
222, 224 are PMOS	**2.** The MOSFET logic circuit as in claim 1, where the second and third transistors are PMOS
221 is NMOS	the first transistor is a NMOS transistor.
A is coupled to 221 and 222	**4.** The MOSFET logic circuit as in claim 1, where the first input signal is provided to a source of the first and second transistors,
B which is an inverse of /B is coupled to the gate of 222	Inverse of the second input signal is provided to a gate of the second transistor, and
/B is coupled to the gate of 221	the second input signal is provided to a gate of the first transistor.
/B is coupled to the gate of 224	**5.** The MOSFET logic circuit as in claim 1 where the second input is provided to a gate of the third transistor.
B is a logic low, the output at 231 is the output of 221 and 222 since 224 is being turned off by /B	**7.** The MOSFET logic circuit as in claim 1 where when the inverse of the second input signal has a logic LOW level, the output of the MOSFET logic circuit is an output signal of the transmission gate.

224 pulls the signal at 321 up to a logic high since its gate voltage /B is logic low, i.e. when the inverse of the second input signal B is a logic high, the second input signal /B is a logic low.	**8.** The MOSFET logic circuit as in claim 1 where the third transistor is a pull-up transistor, and when the inverse of the second input signal has a logic high level, the output of the MOSFET logic circuit has a voltage level approximately equal to a drain of the third transistor, which pulls up the output signal from the transmission gate to a logic high.
delay through 221 and 222 and turn-on delay of 224	**9.** The MOSFET logic circuit as in claim 1, where a delay of the MOSFET logic circuit is one of a delay of the transmission gate formed by first and second transistors and a delay of the third transistor.

5. Claim 10 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Asato (US PAT No. 5,250,855). The response offers that for anticipation to be present each and every element of the claimed invention must be present in a single reference. The examiner agrees; hence:

Fig. 8 of Asato, a logic circuit comprising 83, 84	**10.** A logic OR circuit comprising:
a transmission gate comprising a PMOS transistor designated as T1 ,and a NMOS transistor designated by T2 receiving signals at the	a transmission gate for outputting a first intermediate output signal, the transmission gate being formed by

<table>
<tr><td>by T2 receiving signals at the respective gates outputs Z..
T1 receives A1 at its source and
T2 receives A1 at its source
a gate of T1 receives the inverted output of 82, designated as /B.</td><td>a pMOS transistor receiving a first input signal and
a nMOS transistor receiving said first input signal, where
a gate of the pMOS transistor receives an inverse of a second input signal; and</td></tr>
<tr><td>84 receives the output of 81, B where the outputs of 82 and 81 are the same (col. 5, lines 19-23) since the inputs to the NOR gates 81 and 82 are the same.</td><td>a pull-up pMOS transistor receiving the second input signal,</td></tr>
<tr><td>84 provides an output signal at the node Z by combining the output of T1 and T2 with a signal being pulled up by 84 (see table below)
<table><tr><th>A1</th><th>B</th><th>/B</th><th>83</th><th>84</th><th>Z</th></tr><tr><td>0</td><td>0</td><td>1</td><td>Off</td><td>On</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>On</td><td>Off</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Off</td><td>On</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>On</td><td>Off</td><td>1</td></tr></table></td><td>the pull-up pMOS transistor providing a second intermediate output signal for combining with the first intermediate output signal to create an OR output signal, where the OR output signal is indicative of an OR operation performed on the first and inverse of the second input signals,</td></tr>
<tr><td>the signal at Z is outputted to an inverter (col. 5, lines 30-34).</td><td>the OR output signal is outputted from the OR logic circuit to any static CMOS logic gate.</td></tr>
</table>

Response to Arguments

6. Applicant's arguments filed October 20, 2003 have been fully considered but they are not persuasive. On page 4 of the amendment, applicant argues with respective claims 1-2, 4-5, and 7-9 that "The Sridhar does not teach or describe a circuit that can perform an OR operation between signals A and B' as recited...".

However, the examiner notes that the logic circuit comprising 221, 222, and 224 in Fig. 2g having an output node 231 meets all limitation of the claimed invention, which performs a logic OR operation between A and B which is an inverse of /B as discussed in the rejection of claims.

Applicant further argues that the output table of the inventive circuit is not described by Sridhar.

However, the examiner notes that the output table for Sridhar clearly teaches OR logic operation between A and B (inverse of /B). Regarding amended claim 10, the examiner notes that Fig. 8 of Asato clearly teaches a circuit performing OR logic operation between A and /B as discussed above.

Applicant's arguments with respect to claim 10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory

action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James H. Cho whose telephone number is 703-306-5442. The examiner can normally be reached on Monday-Friday, 05:30am-02:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JHC

December 12, 2003

Jean Bruner Jeanglaude

JEAN JEANGLAUDE
PRIMARY EXAMINER